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PSPLspiceModelsFeb2012.txt
*  SPICE Models for PSPL Coaxial & SMD Components
*  attachment for PSPL Appl.Note, AN-11
*  revision date:  2 Feb 2012
*  PICOSECOND PULSE LABS
*  Jim Andrews, KH6HTV, Maui, Hawaii
*  PSPL Founder & former President (retired)
*  Phenomological spice models for pspl models
*  dc blocks: 5500A, 5501A, 5508, 5509-501,
*             5509-224 & SM-500
*  bias tees: 5541A, 5542, 5542-LL, 5545, 5547,
*             5550B, 5575A, 5580, SM-100, SM-101

*  added Dec 2011, bias tees:  5587, 5589
*  added Feb 2012, bias tees:  5585, 5586
**********************************
.SUBCKT DCB5500 1 2
*  Subcircuit for PSPL model 5500A DC Block
*  0.02uF, 50V, 80kHz- >26GHz
*  J.R.Andrews, PSPL, rev. 8/2/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 25GHz.  Good approx. for IL & RL
C1 1 3 0.02UF  ;  +-20% TOLERANCE
L1 3 4 0.1NH
R2 4 5 6
L2 4 5 0.3NH
R3 5 6 3
L3 5 6 20PH
C3 5 6 75PF
R4 6 7 2
L4 6 7 10PH
C4 6 7 50PF
R5 7 2 470
L5 7 2 27PH
C5 7 2 1.35PF
.ENDS
**********************************
.SUBCKT DCB5501 1 2
*  Subcircuit for PSPL model 5501A DC Block
*  0.22uF, 50V, 7kHz - >26GHz
*  J.R.Andrews, PSPL, 7/30/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 25GHz.  Good approx. for IL & RL
C1 1 3 0.22UF  ;  -50%,+80% TOLERANCE
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R1 3 4 6
L1 3 4 0.18NH
R2 4 5 7
L2 4 5 0.2NH
C2 4 5 14PF
R3 5 2 270
L3 5 2 10PH
C3 5 2 3.75PF
.ENDS
************************************
.SUBCKT DCB5508 1 2
*  Subcircuit for PSPL model 5508 DC Block
*  2.2uF, 16V, 0.7kHz - >26GHz
*  J.R.Andrews, PSPL, 7/31/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 25GHz.  Good approx. for IL & RL
C1 1 3 2.2UF  ;  -50%,+80% TOLERANCE
L1 3 4 0.1NH
R2 4 5 3
L2 4 5 0.1NH
C2 4 5 20PF
R3 5 6 1
L3 5 6 0.1NH
R4 6 7 10
L4 6 7 82PH
R5 7 2 270
L5 7 2 10PH
C5 7 2 3.75PF
.ENDS
*********************************
.SUBCKT DCB5509-501 1 2
*  Subcircuit for PSPL model 5509-501 DC Block
*  500pF, 50V, 3MHz - >50GHz
*  J.R.Andrews, PSPL, 8/7/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 40GHz.  Good approx. for IL & RL
C1 1 3 500PF  ;  +-25% TOLERANCE
L1 3 4 15PH
R2 4 5 0.8
L2 4 5 50PH
R3 5 6 10
L3 5 6 62PH
R4 6 2 1
L4 6 2 1PH
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C4 6 2 28PF
.ENDS
***********************************
.SUBCKT DCB5509-224 1 2
*  Subcircuit for PSPL model 5509-224 DC Block
*  0.22uF, 16V, 7kHz - >50GHz
*  J.R.Andrews, PSPL, rev. 8/7/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 40GHz.  Good approx. for IL & RL
C1 1 3 0.22UF ; -50%, +80% TOLERANCE
L1 3 4 50PH
R2 4 5 0.8
L2 4 5 50PH
R3 5 6 10
L3 5 6 62PH
R4 6 7 2
L4 6 7 1PH
C4 6 7 28PF
R5 7 8 2
L5 7 8 5PH
C5 7 8 20PF
R6 8 2 3
L6 8 2 0.39NH
C6 8 2 560PF
.ENDS
***********************************
.SUBCKT DCBSM500 1 2
*  Subcircuit for PSPL model SM-500 DC Block
*  0.22uF, 16V, 7kHz-35GHz
*  J.R.Andrews, PSPL, 7/31/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 20GHz.  Good approx. for IL & RL
C1 1 3 0.22UF  ;  -50%, +80% TOLERANCE
L1 3 2 0.19NH
C2 3 4 76FF
C3 2 6 76FF
R1 4 0 50
R2 6 0 50
.ENDS
***********************************
.SUBCKT BT5541 1 2 3
*  Subcircuit for PSPL model 5541A bias tee
*  0.02uF,50V,1mH,100mA,3.7ohm,80kHz->26GHz
*  J.R.Andrews, PSPL, rev. 8/2/01
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*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 20GHz.  Good approx. for IL & RL
*  node 1 is AC port, node 2 is AC+DC port
*  node 3 is DC port
*  subckt DCB5500 is required in this model
XC1 1 2 DCB5500  ;  +-20% TOLERANCE
Rdc 2 4 3.7
L1 4 3 1MH  ;       +-20% TOLERANCE
L2 4 5 10UH
R1 5 3 1.8K
R2 3 6 680
C2 6 0 0.01UF
R3 2 7 750
C3 7 8 330PF
R4 8 9 560
L4 8 9 33NH
C4 8 9 0.75PF
R5 9 0 3.3K
L5 9 0 10NH
C5 9 0 375FF
R6 2 10 1.5K
L6 10 11 1UH
C6 11 0 2.5PF
R7 2 12 1K
L7 12 13 500NH
C7 13 0 0.2PF
R8 2 14 560
L8 14 15 200NH
C8 15 0 35FF
.ENDS
***********************************
.SUBCKT BT5542 1 2 3
*  Subcircuit for PSPL model 5542 bias tee
*  0.22uF,16V,1.5mH,100mA,5.6ohm,10kHz->50GHz
*  J.R.Andrews, PSPL, rev. 8/8/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 50GHz.  Good approx. for IL & RL
*  node 1 is AC port, node 2 is AC+DC port
*  node 3 is DC port
C1 1 6 0.22UF  ;    -50%, +80% TOLERANCE
Rdc 2 4 5.6
L1 4 3 1.5MH  ;       +-20% TOLERANCE
R1 4 3 2K
R2 3 5 1K
```

```
C2 5 0 0.22UF
C3 3 0 1NF
R4 2 7 2K
L4 7 8 10UH
C4 8 0 4PF
R5 6 9 3
L5 6 9 0.39NH
C5 6 9 560PF
L6 9 10 50PH
R7 10 2 20
L7 10 2 0.1NH
R8 2 11 75
L8 11 12 0.68NH
C8 12 0 10FF
R9 2 13 500
L9 13 14 33NH
C9 14 0 0.75FF
R10 2 15 750
L10 15 16 22NH
C10 16 0 12FF
.ENDS
************************************
.SUBCKT BT5542LL 1 2 3 4
*  Subcircuit for PSPL model 5542-LL bias tee
*  0.22uF,16V,1.5mH,100mA,5.6ohm,12kHz->40GHz
*  this bias tee has 2 dc ports
*  J.R.Andrews, PSPL, 8/8/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 40GHz.  Good approx. for IL & RL
*  node 1 is AC+DC port, node 2 is AC+DC port
*  node 3 is DC port #1 connected to node 1
*  node 4 is DC port #2 connected to node 2
C5 1 9 0.22UF  ;    -50%, +80% TOLERANCE
Rdc1 1 5 5.6
L1 5 3 1.5MH  ;       +-20% TOLERANCE
R1 5 3 2K
R3 3 6 1K
C1 6 0 0.22UF
C3 3 0 1NF
Rdc2 2 7 5.6
L2 7 4 1.5MH  ;       +-20% TOLERANCE
R2 7 4 2K
R4 4 8 1K
C2 8 0 0.22UF
C4 4 0 1NF
```

```
R6 9 10 3
L6 9 10 0.39NH
C6 9 10 560PF
L7 10 11 82PH
R8 11 2 20
L8 11 2 68PH
R9 2 12 1K
L9 12 13 5UH
C9 13 0 8PF
R10 2 14 68
L10 14 15 0.43NH
C10 15 0 16FF
R11 2 16 100
L11 16 17 2.7NH
C11 17 0 4.7FF
R12 2 18 1.2K
L12 18 19 33NH
C12 19 0 12FF
R13 2 20 1K
L13 20 21 68NH
C13 21 0 0.65FF
R14 2 22 1K
L14 22 23 68NH
C14 23 0 0.41FF
.ENDS
**********************************
.SUBCKT BT5545 1 2 3
*  Subcircuit for PSPL model 5545 bias tee
*  0.03uF,50V,340uH,500mA,1.1ohm,65kHz->20GHz
*  J.R.Andrews, PSPL, 8/2/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 20GHz.  Good approx. for IL & RL
*  node 1 is AC port, node 2 is AC+DC port
*  node 3 is DC port
C1 1 16 0.03UF  ;  +-20% TOLERANCE
Lcap 16 17 0.22NH
L9 17 2 0.15NH
C9 17 18 60FF
C10 2 19 60FF
R9 18 0 50
R10 19 0 50
Rdc 2 4 1.1
L1 4 3 340UH  ;  +-20% TOLERANCE
L2 4 5 1UH
R1 5 3 2.2K
```

```
R2 3 6 430
C2 6 0 0.22UF
R3 2 7 470
C3 7 8 220PF
R4 8 9 470
L4 8 9 33NH
C4 8 9 0.33PF
R5 9 0 150
L5 9 0 4.7NH
C5 9 0 0.33PF
R6 2 10 1K
L6 10 11 330NH
C6 11 0 0.3PF
R7 2 12 470
L7 12 13 220NH
C7 13 0 15FF
R8 2 14 220
L8 14 15 22NH
C8 15 0 3.5FF
.ENDS
************************************
.SUBCKT BT5547 1 2 3
*  Subcircuit for PSPL model 5547 bias tee
*  0.44uF,50V,1.34mH,500mA,1.5ohm,5kHz-15GHz
*  J.R.Andrews, PSPL, 8/2/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 20GHz.  Good approx. for IL & RL
*  node 1 is AC port, node 2 is AC+DC port
*  node 3 is DC port
C1 1 10 0.44UF ; -50%,+80% TOLERANCE
Lcap 11 2 0.1NH
R4 10 11 18
L4 10 11 0.47NH
Rdc1 2 4 1.1
L1 4 7 340UH  ;  +-20% TOLERANCE
L2 4 5 4.7UH
R1 5 7 2.2K
R2 7 6 820
C2 6 0 0.22UF
R3 2 9 430
C3 9 0 3.3NF
* if the ext. coil is not used, then delete
* Lx,Rx & Rdcx and instead use
* Rdcx 7 3 0.01
Lx 7 8 1MH  ;   +-30% TOLERANCE
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```
Rx 7 8 430
Rdcx 8 3 0.4
.ENDS
************************************
.SUBCKT BT5550 1 2 3
*  Subcircuit for PSPL model 5550B bias tee
*  0.02uF,50V,1mH,50/500mA,0.4ohm,100kHz-18GHz
*  J.R.Andrews, PSPL, 8/3/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 20GHz.  Good approx. for IL & RL
*  node 1 is AC port, node 2 is AC+DC port
*  node 3 is DC port
*  subckt DCB5500 is required in this model
XC1 1 6 DCB5500  ;  +-20% TOLERANCE
Rdc 6 4 0.4
L1 4 3 1MH  ;       +-30% TOLERANCE
R1 4 3 1.5K
R2 6 5 270
C2 5 0 5NF
C3 7 0 0.27PF
L2 7 8 0.68NH
C4 8 0 0.27PF
R3 6 7 12
L3 6 7 68PH
R4 8 2 12
L4 8 2 68PH
.ENDS
**********************************
.SUBCKT BT5575 1 2 3
*  Subcircuit for PSPL model 5575A bias tee
*  0.22uF,50V,1mH,20/500mA,0.6ohm,10kHz-12GHz
*  J.R.Andrews, PSPL, 8/3/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 20GHz.  Good approx. for IL & RL
*  node 1 is AC port, node 2 is AC+DC port
*  node 3 is DC port
*  subckt DCB5501 is required in this model
XC1 1 6 DCB5501  ;  -50%, +80%% TOLERANCE
Rdc 6 4 0.6
L1 4 3 1MH  ;       +-30% TOLERANCE
R1 4 3 2.2K
R2 6 5 390
C2 5 0 0.01UF
R3 2 7 120
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```
L3 7 8 5NH
C3 8 0 36FF
R4 2 9 120
L4 9 10 3.3NH
C4 10 0 33FF
C5 6 0 0.29PF
L5 6 2 0.72NH
C6 2 0 0.29PF
.ENDS
************************************
.SUBCKT BT5580 1 2 3
*  Subcircuit for PSPL model 5580 bias tee
*  0.22uF,50V,1mH,1 Amp,0.8ohm,10kHz-15GHz
*  J.R.Andrews, PSPL, 8/4/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 20GHz.  Good approx. for IL & RL
*  node 1 is AC port, node 2 is AC+DC port
*  node 3 is DC port
C1 1 6 0.22UF  ;  -50%, +80%% TOLERANCE
Rdc 6 4 0.8
L1 4 3 1.1MH  ;       +-25% TOLERANCE
R1 4 3 3.3K
R2 6 5 220
C2 5 0 0.05UF
R3 6 7 180
L3 7 8 33NH
C3 8 0 30FF
R4 6 9 110
L4 9 10 4.7NH
C4 10 0 43FF
R5 6 11 150
L5 11 12 3.3NH
C5 12 0 27FF
C6 6 0 0.29PF
L6 6 2 0.72NH
C7 2 0 0.29PF
.ENDS
************************************
.SUBCKT BTSM100 1 2 3
*  Subcircuit for PSPL model SM-100, SMD, bias tee
*  0.22uF,16V,470uH,500mA,2.8ohm,14kHz-13GHz
*  J.R.Andrews, PSPL, 8/4/01, rev. 8/6/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 20GHz.  Good approx. for IL & RL
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*  node 1 is AC port, node 2 is AC+DC port
*  node 3 is DC port
*  subckt DCBSM500 is required in this model
XC1 1 8 DCBSM500  ; -50%, +80% TOLERANCE
Rdc 8 4 2.8
L1 4 3 470UH  ;       +-25% TOLERANCE
L2 4 5 2.2UH
R1 5 3 3K
R2 3 6 1K
C2 6 0 0.01UF
R3 8 7 1.2K
C3 7 0 330PF
C4 8 0 0.22PF
L4 8 2 1.0NH
C5 2 0 0.22PF
.ENDS
**********************************
.SUBCKT BTSM101 1 2 3
*  Subcircuit for PSPL model SM-101, SMD, bias tee
*  0.22uF,16V,2.9uH,500mA,1.4ohm, 15GHz BW
*  -3dB LF = 7kHz (dc=hi-z) or 1.4MHz (dc=lo-z)
*  J.R.Andrews, PSPL, 8/6/01
*  This is NOT the actual circuit -- but a
*  phenomological model.  Model not valid for
*  f > 20GHz.  Good approx. for IL & RL
*  node 1 is AC port, node 2 is AC+DC port
*  node 3 is DC port
*  subckt DCBSM500 is required in this model
XC1 1 8 DCBSM500  ; -50%, +80% TOLERANCE
Rdc 8 4 1.4
L1 4 3 2.9UH  ;       +-25% TOLERANCE
L2 4 5 0.3UH
R1 5 3 1.2K
R2 3 6 470
C2 6 0 1NF
R3 8 7 1.8K
C3 7 0 1PF
C4 8 0 0.2PF
L4 8 2 0.85NH
C5 2 0 0.2PF
.ENDS
**********************************
.SUBCKT BT5585 1 2 3
*  Subcircuit for PSPL model 5586 bias tee
*  5585 KEY SPECS:  2-18GHz (-1dB BW),  Cac = 1nF, L = 6nH, Cbp = 2nF
*  PICOSECOND PULSE LABS
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*  Jim Andrews, KH6HTV, 27 Jan 2012
*  This is NOT the actual circuit -- but a phenomological model.
*  Fair approximation for IL & RL
*  Valid for f < 20 GHz
*  node 1 is AC port, node 2 is AC+DC port,  node 3 is DC port
*C1 1 2 1NF ; DC blocking capacitor
*C2 3 0 2NF ; DC input by-pass capacitor
*L1 3 2 6NH ; DC feed inductor
* model for C1, DC blocking capacitor
C1 1 4 1nF ; DC blocking capacitor
RC1 4 6 0.5
LC1 4 6 0.1NH
L2C1 6 2 0.2NH
* model for C2, DC input bypass
C2 3 5 2NF
RC2 5 0 1
LC2 5 0 0.1NH
* model for 6nH DC feed inductor
TLA  2 0 10 0 Z0=350 TD= 3.7PS
TLB 10 0 12 0 Z0=350 TD= 3.7PS
TLC 12 0 14 0 Z0=350 TD= 3.7PS
TLD 14 0 16 0 Z0=350 TD= 3.7PS
TLE 16 0 18 0 Z0=350 TD= 3.7PS
TLF 18 0 20 0 Z0=350 TD= 3.7PS
RLA 10 11 2K
CLA 11 0 0.05PF
RLB 12 13 2K
CLB 13 0 0.05PF
RLC 14 15 2K
CLC 15 0 0.05PF
RLD 16 17 2K
CLD 17 0 0.05PF
RLE 18 19 2K
CLE 19 0 0.05PF
RLF 20 21 2K
CLF 21 0 0.05PF
RL1dc 20 3 0.01
.ENDS
************************************************
.SUBCKT BT5586 1 2 3
*  Subcircuit for PSPL model 5586 bias tee
*  5589 KEY SPECS:  1 - 5GHz (-1dB BW),  Cac = 1nF, L = 15nH, Cbp = 22nF
*  PICOSECOND PULSE LABS
*  Jim Andrews, KH6HTV, rev. 2 Feb 2012
*  This is NOT the actual circuit -- but a phenomological model.
*  Fair approximation for IL & RL
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*  Valid for f < 5.5 GHz, does not model depth of first notch accurately
*  node 1 is AC port, node 2 is AC+DC port,  node 3 is DC port
C1 1 5 1nF ; DC blocking capacitor
RC1 5 2 2 ;  loss in C1 to provide mid-band (1.5GHz) insertion loss
C2 3 6 22nF ; DC input by-pass capacitor
RC2hf 6 0 0.5 ; hf loss in by-pass cap to model isolation
TL1 2 0 4 0 Z0=200 TD=85.5PS ; model for 51nH DC feed inductor  *L1 2 4
15nH
RL1dc 4 3 0.01 ; DC resistance of 15nH inductor
.ENDS
*********************************************
.SUBCKT BT5587 1 2 3
*  Subcircuit for PSPL model 5587 bias tee
*  5587 KEY SPECS:  0.2 - 2GHz (-1dB BW),  Cac = 1nF, L = 88nH, Cbp = 22nF
*  PICOSECOND PULSE LABS
*  Jim Andrews, KH6HTV, 12/23/2011
*  This is NOT the actual circuit -- but a phenomological model.
*  Good approximation for IL & RL
*  Valid for f < 3 GHz
*  node 1 is AC port, node 2 is AC+DC port,  node 3 is DC port
C1 1 5 1nF ;    DC blocking capacitor
RC1 5 2 0.6 ;   loss in C1 to provide mid-band (1.5GHz) insertion loss of
0.05dB
C2 6 0 22nF ;   DC input by-pass capacitor
RC2hf 3 6 0.5 ; hf loss in by-pass cap to model isolation
TL1 2 0 4 0 Z0=400 TD=231.2PS ; model for 51nH DC feed inductor  *L1 2 4
88nH
RL1dc 4 3 0.02 ;  DC resistance of 51nH inductor
.ENDS
*
*********************************************
.SUBCKT BT5589 1 2 3
*  Subcircuit for PSPL model 5589 bias tee
*  5589 KEY SPECS:  0.3-2.8GHz (-1dB BW),  Cac = 1nF, L = 51nH, Cbp = 22nF
*  PICOSECOND PULSE LABS
*  Jim Andrews, KH6HTV, rev. 12/23/2011
*  This is NOT the actual circuit -- but a phenomological model.
*  Good approximation for IL & RL
*  Valid for f < 4 GHz
*  node 1 is AC port, node 2 is AC+DC port,  node 3 is DC port
C1 1 5 1nF ; DC blocking capacitor
RC1 5 2 0.6 ;  loss in C1 to provide mid-band (1.5GHz) insertion loss of
0.05dB
C2 6 0 22nF ; DC input by-pass capacitor
RC2hf 3 6 0.5 ; hf loss in by-pass cap to model isolation
TL1 2 0 4 0 Z0=400 TD=161.7PS ; model for 51nH DC feed inductor  *L1 2 4
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51nH
RL1dc 4 3 0.015 ; DC resistance of 51nH inductor
.ENDS
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