Picosecond Pulse Labs

Application Note AN-19

Picosecond Pulse Generation Techniques & Pulser Capabilities

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Table I PSPL Pulse Generator & Pulse Amplifier Capabilities

Risetimes	Amplitudes	Rep. Rate	Technique	Example Models
2.5 ns	20 V	165MHz	discrete Silicon RF Transistor	12000
250 ps	50 V	100 kHz	Avalanche Transistor	10300B
125 ps	2.5 V	1.6 GHz	custom design MMIC	12020
100 ps	35 V	100 kHz	Step Recovery Diode	4500E
45 ps	10 V	100 kHz	Step Recovery Diode	10050A
25 ps	8 V	12 GHz	custom design MMIC	5865
20 ps	250 mV	50 kHz	Tunnel Diode	TD1107
20 ps	2 V	25 GHz	custom design MMIC	PPA
8 ps	2.5 V	45 GHz	custom design MMIC	5882
< 5 ps	5 V	500 kHz	PSPL Non-Linear Transmission Line	4016

Since it's founding in 1980, Picosecond Pulse Labs (PSPL) has specialized in the 'niche' market area of building ultra-fast risetime (down to 5 ps) and high amplitude (up to 50 V) pulse generators. The unique combination of both fast risetime and high amplitudes simultaneously has required the use of several non-conventional techniques. Table I above gives a brief overview of the capabilities of various pulse generation techniques used by PSPL. The four techniques of discrete RF transistor, avalanche transistor, step-recovery diode and tunnel diode are classical and can be found in the scientific literature dating back to the 1960s. They have been used by PSPL since its earliest days in the 1980s. More recently PSPL has added the ability of making it's own semiconductors resulting in the addition of custom designed Non-Linear Transmission Lines (NLTL) and analog/digital Monolithic Microwave Integrated Circuits (MMIC). Figures 1-3 show the performance of some of PSPL's newer products using NLTL and MMIC technologies.

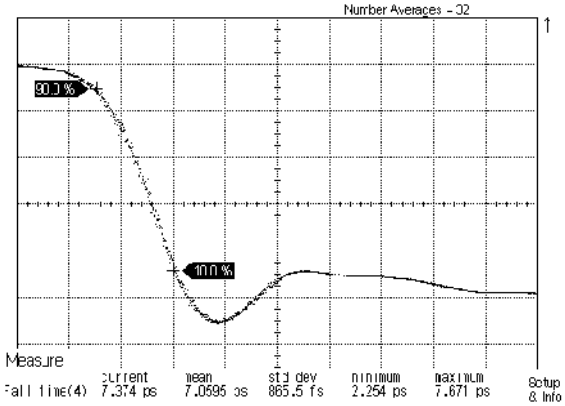

Fig. 1 PSPL model 4016, < 5 ps falltime, -5 V NLTL pulse, at 1 V/div & 5 ps/div measured on PSPL 100 GHz sampler

Fig. 1 shows the < 5 ps, -5 V NLTL pulse from the world's fastest, commercially available, pulse

generator, the PSPL model 4016, as measured on PSPL's 100 GHz sampling oscilloscope. After deconvolving the risetime contributions from the sampler, coax adapter, coax attenuator and timing jitter, the actual generator's falltime was estimated to be 3 ps. PSPL 100 GHz sampling heads along with lower bandwidth electrical and optical sampling heads made by PSPL are available from LeCroy. (www.lecroy.com)

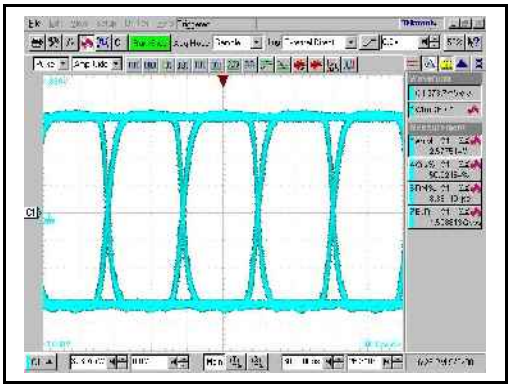

Fig. 2 PSPL, custom MMIC, model 12020 Pulse/Pattern Generator 2.5 V, 1.6 GHz, 125 ps rise/fall, PRBS, NRZ eye diagram, 300 ps/div

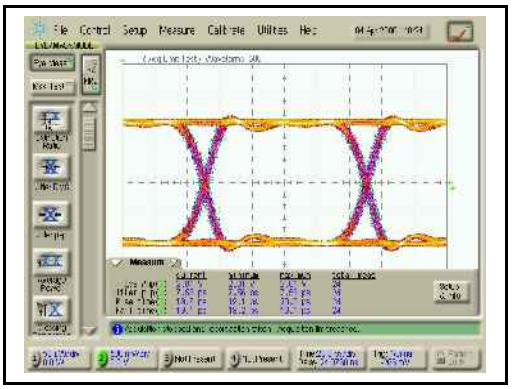

Fig. 3 PSPL, custom MMIC, Programable Pattern Amplifier 10 GHz PRBS, NRZ eye diagram 0.5 V/div & 20 ps/div

Fig. 2 shows the capability of one of PSPL's newest, general purpose, programmable pulse/pattern generators to produce very high quality data eye diagrams with 125 ps rise/falltimes. It uses PSPL custom MMICs. In addition to generating PRBS patterns, the generators can produce programmable data words and perform as classical pulse generators with adjustable rep. rate, delay, duration, polarity, amplitude and offset. They also include a unique new feature of adjustable jitter insertion.

PSPL also builds a line of very high performance amplifiers which when driven by pulse or data sources provide metrology grade quality performance. The dc coupled PSPL Programable Pattern Amplifier's (PPA) performance is shown in Fig. 3. It is capable of producing 2 V amplitude, 20 ps rise/falltime pulses and data patterns at clock rates up to 25 GHz.

SILICON TRANSISTORS

Conventional, discrete, silicon transistors have been used since the early 1960s to perform switching and amplifier functions. To generate fixed risetime pulses, RF transistors are usually used in a switching (on / off) mode. To avoid saturation effects, which slow recovery time and limit the max. rep. rate, the most common circuit arrangement used is an emitter coupled differential pair as the output stage of a pulse generator, Fig. 4. The transistors, Q1 & Q2 are emitter fed by a constant current source and they are either on in the linear region or turned off. They are not allowed to saturate in the on state. True and compliment outputs are available. The

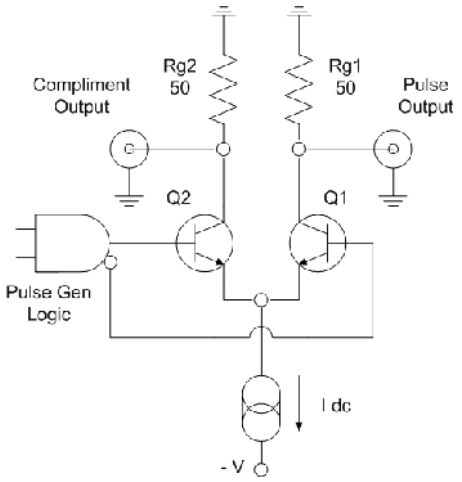

Fig. 4 Emitter coupled transistor output stage to generate fixed rise/falltime pulses. (*)

(*) Circuit diagrams shown in this application note are only intended to convey general concepts. They are not the actual circuits used in PSPL products.

collector resistors, R_{g1} & R_{g2} set the generator's output impedance and are typically 50 Ω With conventional, discrete, Si RF power transistors, 2 V pulses (into 50 Ω) with 1.5 ns rise/falltimes can easily be achieved.

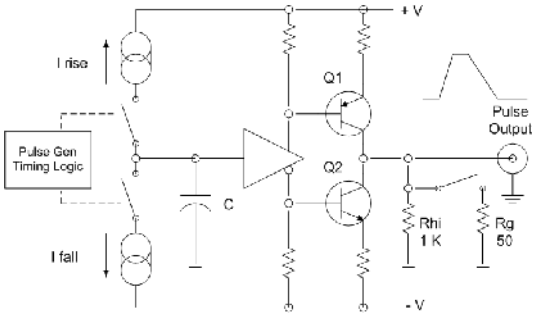

Fig. 5 Ramp generator & linear amplifier to generate adjustable rise/falltime pulses.

For adjustable risetime pulses (> 2 ns rise/fall), it is necessary to instead use a linear amplifier as the output stage of a pulse generator. The adjustable, linear rising and falling edges are created by charging and discharging a capacitor with constant current sources. See Fig. 5 above. $V_c = 1/C * \int i(t) * dt$ Decade changes in rise/fall time are set by selecting various timing capacitors. Fine adjustments in rise/falltime are made by adjusting the constant current sources.

The voltage across the ramp generator capacitor, C, is then amplified / buffered by the output, linear, transistor amplifier. The output PNP & NPN transistors, Q1 & Q2 are operated as high output impedance, constant current sources. The output impedance is then set by the shunt resistor, R_{hi} (typically 1 KΩ) or R_g (50 Ω). Adjustable pulse rise/falltimes as fast as 2.5 ns, at max. rep. rates of 165 MHz, can be generated with this technique along with pulse amplitudes up to 10 V into 50 Ω. If the generator source resistor, R_g , is switched out, then pulse amplitudes up to 20 V into 50 Ω can be generated. The balance of the pulse generator circuitry to determine the rep. rate, delay, duration, rise/fall control, etc. is usually implemented with conventional TTL or ECL logic ICs.

The PSPL Model 12,000 programmable, 165 MHz, Pulse/Pattern Generator uses this technique.

This adjustable rise/falltime generation technique is not readily scalable to faster risetimes. Pulse generators presently offered by all manufacturers with rise/falltimes less than about 1 ns have fixed edge speeds. To have adjustable, < 1 ns, rise/falltimes requires placing a low-pass filter on the generator's pulse output to slow down it's edge speeds. For proper, clean, pulse response, a low-pass filter must have a Gaussian time and frequency response. The relationship between risetime (10-90%) and bandwidth (-3dB) for a Gaussian network is given by Tr * BW = 0.35. For additional information on Risetime Filters, see PSPL's Application Note, AN-7a, "*Low-Pass, Risetime Filters for Time Domain Applications*". PSPL offers a very complete selection of Risetime (Low-Pass) Filters. The PSPL 5900 series of filters have risetimes ranging from 12 ps to 10 ns and corresponding bandwidths from 28 GHz to 35 MHz. In addition to standard values, PSPL can also build custom ordered values.

AVALANCHE TRANSITORS

Avalanche breakdown in bi-polar transistors is a phenomena that most circuit designers really want to avoid. However, if harnessed properly, it can be used to generate relatively high pulse voltages of 50 to 100 Volts with sub-nanosecond risetimes.

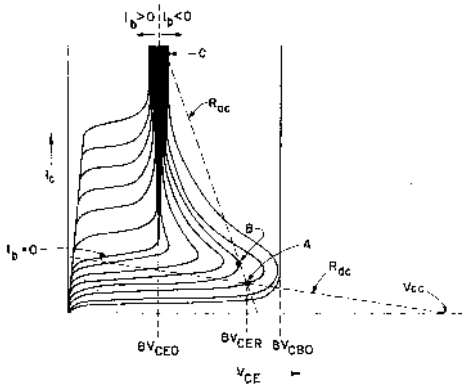

Fig. 6 Avalanche transistor I - V curve

Avalanche multiplication in reverse-biased pn junctions is a result of impact ionization produced by mobile charge carriers. If the electric field in the depletion region of the pn junction is large enough, an electron moving through the crystal lattice gains sufficient energy to release an additional electron and hole when it collides with an atom in the lattice. The two free electrons may then cause additional ionizations

and an ever-growing cascade, or an avalanche of ionization occurs.

In transistors the avalanche breakdown may be controlled through the injection of carriers by the base current, Fig. 6. Normal transistor operation lies in the region of collector-emitter voltages between 0 and BV_{ceo} and forward base currents. BV_{ceo} is the breakdown voltage from the collector to the emitter with the base open circuited. If a reverse base current is applied, then the collector-emitter voltage may be increased above BV_{ceo} before an avalanche breakdown is reached. The upper voltage limit, BV_{cbo}, is reached when $I_b = I_c$. BV_{cbo} is the breakdown voltage from the collector to the base with the emitter open circuited. The avalanche region of the transistor lies between BV_{ceo} and BV_{cbo}. An important item to notice in Fig. 6 is the negative slope of the constant I_b curves in the avalanche region. The negative slope means that the small-signal resistance, $r_a = dV/di$, is negative. A negative resistance implies unstable operation. Thus the avalanche transistor is useful as an oscillator or switching element. The switching speeds that can be obtained are quite fast because of the multiplying effect of the avalanche breakdown.

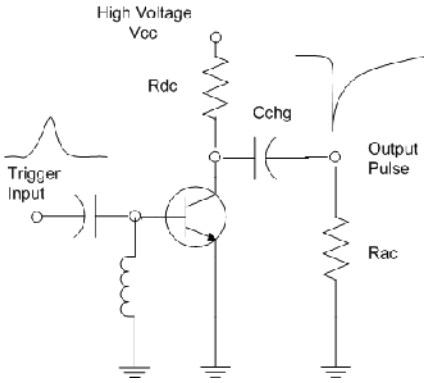

Fig. 7 Avalanche Pulse Generator

A typical avalanche transistor switching circuit is shown in Fig. 7. The large supply voltage, V_{cc}, and the dc load resistor, R_{dc} place the transistor at the stable operating point A, Fig. 6. Note the dc load line labeled R_{dc}. The inductor provides a dc short between the base and the emitter and a path for the negative leakage base current to flow. In the dc quiescent state, only a few μa of current are flowing in the transistor. The charging capacitor, C_{chg}, is however charged up to the voltage BV_{cer} noted at point A.

A positive polarity trigger pulse AC coupled into the base increases the base current causing the collector current to move along the ac load line, R_{ac}, to operating point B. Point B is in the negative resistance region and is an unstable point. Thus the operating point rapidly switches along the ac load line to the next stable location, point C. With dramatic differences in ac vs. dc load lines (typically < 50 Ω vs. > 100 kΩ), the currents flowing in the transistor rapidly switch from a few μa to potentially several Amps when capacitor C_{chg} discharges through R_{ac} and the transistor.

The simple circuit shown in Fig. 7 generates a negative polarity, exponential pulse with a fast falltime and a slow, exponential rise on the trailing edge. The time constant of the pulse trailing edge is set by $\tau_p = R_{ac} * C_{chg}$. The pulse amplitude is $V_p = BV_{cer} - BV_{ceo}$. Rectangular pulses can be generated if the charge capacitor is replaced by a coaxial transmission line.

The max. possible rep. rate of an avalanche transistor pulser is severely limited by two constraints. The first is the requirement to recharge the capacitor. The recharge time constant is much larger than the pulse time constant. $\tau_{chg} = R_{dc} * C_{chg}$. The second limitation is due to the power handling capability of the transistor. When the transistor goes into avalanche breakdown, the collector voltage does not drop to zero. Instead it drops to a lower breakdown voltage, BV_{ceo}. Thus during breakdown with high current flowing, the peak power dissipated in the transistor is extremely high. To stay within the transistor's average power rating, the pulse duty cycle must be kept very low with the trigger input rep. rate severely limited to a few kHz

Several PSPL pulse generator models use avalanche transistors to generate high amplitude, sub-ns pulses. They include: model 1000D, ± 35 V, 500 ps impulse generator and the model 2600C which generates ± 50V, 250ps risetime, rectangular pulses which are adjustable in duration from 1 ns to 100 ns. The model 10,300B is a GPIB programmable version of the 2600C.

STEP-RECOVERY DIODE

The Step-Recovery Diode (SRD) is a special microwave, semiconductor diode. Fig. 8 shows a typical SRD pulse generating circuit. An SRD is mounted in shunt across a 50 Ω line. It is forward biased with a constant current source through an RF choke.. Two dc blocking capacitors are used to force all of the bias current through the SRD. The SRD is strongly turned on by the forward bias current and it's P-N juction is full of a lots of charge carriers. When

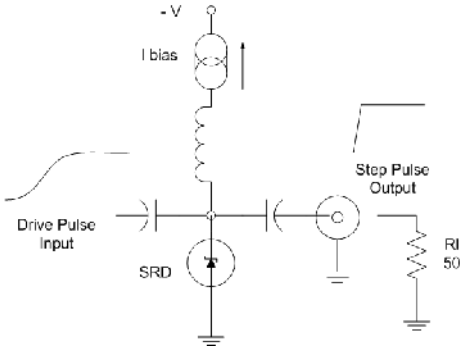

Fig. 8 SRD pulse generator

a large drive pulse is applied to the SRD, it attempts to turn-off the SRD. Due to the charge carriers stored in the P-N junction, the current flow doesn't stop immediately, but instead reverses direction until all of the charge carriers in the P-N junction are depleted. During this 'reverse-recovery' interval, the SRD is still conducting and acts as a low impedance shunt across the 50 Ω line, thus preventing most of the drive pulse from propagating towards the output load, R_l. When all of the charge carriers in the P-N junction are depleted, the SRD then rapidly returns to it's non-conducting, reverse biased state. When this happens, all of the drive pulse can then pass un-impeded on to the output load, R_l. This reverse recovery time phenomena occurs in almost all semiconductor diodes (except Schottkys). However, the doping profiles in SRDs have been optimized to sweep all of the charge carriers out at the same instant and thus they have an extremely abrupt turn-off edge. SRD pulsers are capable of generating 35 V pulses with 100 ps edges down to 10 V pulses with 50 ps edges. The drive pulse in PSPL SRD pulsers is usually generated by an avalanche transistor. Thus the max. rep. rates possible with PSPL SRD pulsers is limited by the avalanche transistor driver.

Several PSPL pulse generators use SRDs to generate sub 100 ps risetime pulses. These generators include: model 4500E, 35V, 100 ps rise; model 4050B, 10 V, 45 ps rise; and model 3500D, ± 8V, 65 ps wide impulse. The models 10,050A, 10,060A, and 10,070A are GPIB programmable versions of the 4050B.

TUNNEL DIODE

The Tunnel Diode (TD) is a very specialized diode with a highly unusual I - V characteristic. See Fig. 9. The "tunneling" phenomena was discovered in the early 60s. Tunnel diodes were the first semiconductor device capable of operating as oscillators, amplifiers and switches at microwave frequencies. By the mid-60s, both Hewlett-Packard and Tektronix had introduced pulse generators capable of risetimes as fast as 25 ps using germanium tunnel diodes.

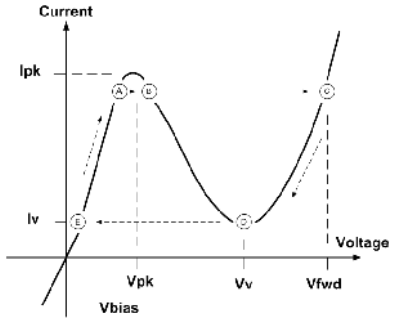

Fig. 9 Tunnel Diode I - V Curve

A tunnel diode behaves like an ordinary diode with a strong exponential I-V curve in the strongly forward biased region (quadrant I). In the reverse bias condition (quadrant III), it doesn't have a typical diode, non-conducting state. Instead, it acts like a low value resistor. In the low voltage, forward bias region (quadrant I), it has a peculiar "S" shaped curve. The intermediate region of the "S" I-V curve has a negative slope, which implies a negative resistance, $R_{td} = dV/di$

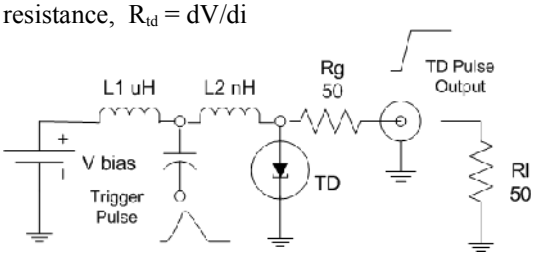

Fig. 10 Tunnel Diode Pulse Generator

Fig. 10 is a simple TD pulse generator circuit. It can be used to describe the basic operation of a

TD to generate fast pulses. A very stable, low voltage, bias source is used to bias the TD to point A on the I-V curve. Point A is set perhaps 1% below the peak point current, I_{pk}, of the TD. For ac purposes, this bias voltage is isolated from the TD by a large inductor, L_1. A positive triggering pulse is coupled to the TD via capacitor C and a small inductor, L_2. The extra triggering current causes the TD current to exceed I_{pk} and pushes the operating point "over the top" to point "B". Point "B" is in the negative resistance region and is unstable. Thus, instead of remaining at "B", because the diode is being fed with a constant current (due to L1), the TD's operating point rapidly switches to the stable operating point "C". In doing so, the voltage across the TD suddenly experiences a sizeable voltage jump, ΔV. For Ge TDs, this is about ½ V. The "tunneling" phenomena inside the TD junction is essentially instantaneous. The TD terminal voltage transient conditions are determined by the diode's junction capacitance and it's peak current rating. The diode's switching time can be estimated closely by the simple equation: $\Delta T_{td} = (C_{td} * \Delta V) / I_{pk}$ where $\Delta V = V_C - V_A$

During the TD's switching time, the small nH inductor, L_2, forces all of the voltage pulse energy to travel towards the right to the pulse generator output. The TD's effective impedance is quite low when it is at point "C". Thus, a series resistor, Rg, is used to set the output impedance of the generator to 50 Ω. The output voltage into the external 50 Ω load is about ½ * ΔV.

With a large μH inductor used for L_1, it will continue to push a constant current of I_{pk} through the TD for a few μs, thus creating a long flat-top, step-like pulse. Eventually, however, L_1 can't maintain this current indefinitely and the operating point eventually starts to slide down the I-V curve to point "D". When it reaches "D", the TD again enters its unstable region and now rapidly switches to the new stable operating point "E". From "E" the current through L_1 slowly increases until the TD once again reaches its stable, initial operating point "A" set by the dc bias voltage source.

If point "A" were to be biased into the negative resistance region, this circuit would operate as an oscillator rather than a triggered pulser. The oscillation period, or the pulser recovery time, is determined by the size of the inductors L_1 & L_2. TDs are capable of oscillating at microwave frequencies under the proper circuit conditions.

One of PSPL's very earliest pulse generators used tunnel diodes to generate 250 mV, 20 ps risetime pulses. It is the model TD-1107C Pulse Head. The companion bias and trigger source driver for the TD-1107 is the TD-1110D.

NON-LINEAR TRANSMISSION LINE

The technique capable of generating the fastest risetime, electrical pulses uses a Non-Linear Transmission Line (NLTL). To understand the behavior of an NLTL, it is first necessary to review the basic characteristics of a transmission line. The equivalent circuit model for a transmission line is shown in Fig. 11. It consists of a distributed network of infinitely small series inductors, ΔL (μH/cm) and shunt capacitors, ΔC (pF/cm). The characteristic impedance, Z_0 is given by the equation: $Z_0 = (\Delta L / \Delta C)^{1/2}$ The time delay, TD_{ul}, per unit length is given by: $TD_{ul} = (\Delta L * \Delta C)^{1/2}$ An ideal, loss-less, transmission line will have a resistive characteristic impedance, an infinite bandwidth and a non-frequency dependent time delay. i.e. no phase shift, except for a fixed delay.

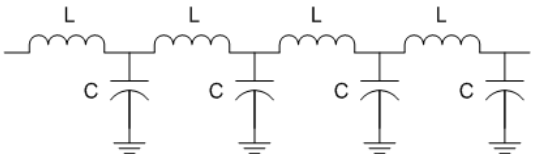

Fig. 11 Transmission Line Model

An artificial transmission line can be built using discrete elements for the series inductors and shunt capacitors. It will exhibit the same behavior of a characteristic impedance, Z_0, and time delay, TD_{LC} (per unit LC element) as given by the above equations. The time delay for an artificial line built with "*n*" number of identical sections is approximately $TD_{al} = n * (L*C)^{1/2}$ However, it will not have an infinite bandwidth and will have a strongly frequency dependent phase shift. The artificial transmission line is in reality a low-pass filter. Each LC element has an upper frequency cutoff of $f_0 = 1 / [2\pi (L*C)^{1/2})]$ The risetime of a single LC section is $t_{rss} = 1.13 (L*C)^{1/2}$ For a cascade of "*n*" sections, the composite risetime is $(n)^{1/3} * t_{rss}$. In addition, a simple artificial transmission line

will exhibit a lot of ringing on its pulse step response.

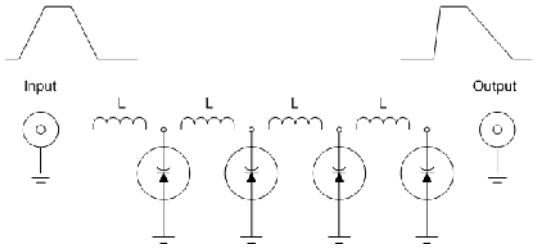

Fig. 12 Non-Linear Transmission Line

A Non-Linear Transmission Line, NLTL, is built using either non-linear inductors, L(i), or capacitors C(V), whose values are a function of either the current, i, or voltage, V. Fig. 12 shows an example of using non-linear capacitors. In this case, the non-linear capacitors are varactor diodes. A varactor diode is a special diode with a doping profile designed to give a strong variation in diode capacitance as a function of applied reverse voltage. To generate fast risetime pulses, the key phenomena to be utilized in an NLTL will be the strongly voltage dependent time delay. For an NLTL built with "N" stages, the overall time delay will be: $TD = N * [L * C_v(V)]^{1/2}$ Fig. 13 shows a typical plot of relative time delay vs. voltage for a PSPL NLTL.

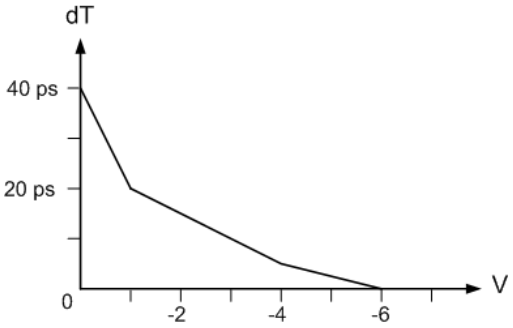

Fig. 13 Typical NLTL time delay shift vs. voltage

For a positive polarity NLTL, as shown in Fig. 12, with the varactor diodes reverse biased, an applied positive pulse voltage with a slow risetime will experience a delay in the leading edge followed by a "sharpening", or speeding up of the risetime. This can be explained as follows: For the low voltage portion of the drive waveform, the pulse experiences a lot of time delay. As the pulse voltage rises, it experiences progressively less and less time delay, resulting in a faster risetime. On the trailing edge of the pulse however the opposite effect occurs, with the falltime becoming slower. In the ideal situation, the risetime of the input drive pulse will match the ΔTD of the NLTL. As a first approximation, the output risetime is given by: $T_{rout} = T_{rin} - \Delta TD_{nltl}$ As an example for 100 ps input and a 60 ps NLTL, T_{rout} = 100ps - 60ps = 40ps. There is however a finite limit to the pulse sharpening effect. If for example, the input risetime were 60 ps, the output would not be T_{rout} = 60ps - 60ps = 0ps ! ! ! The NLTL has the same bandwidth / risetime limitations as the lumped element artificial line described above. As an example, one of PSPL's fastest NLTLs will compress a pulse by 25 ps but has a limiting risetime of 4 ps.

Several PSPL pulse generators use NLTLs designed and built by PSPL. They include the model 3600 impulse generator (70ps, -7.5V, 2.5 GHz), and step generators: model 4015D (12 ps, -5 V), model 4005 (9 ps, +5 V) and the 4016 (<5 ps, -5 V). See Fig. 1 for the 4016's NLTL pulse leading edge waveform. These step generators require < 50 ps drive pulses which are generated using some of the other technologies discussed in this application note. NLTLs are also used in PSPL's ultra-wideband (up to 100 GHz) sampling heads as the sampling strobe drivers. For additional details on PSPL's NLTLs, see the PSPL Application Note, AN-13, "*Driving and Biasing PSPL's Edge Compressor Components*".

CUSTOM MMIC

During PSPL's early years in the 80s & 90s, all PSPL products were designed and built around using commercial, off-the-shelf, electronic components. For some particularly, ultra-fast pulse generators, pre-screening, hand selection of critical components, and hand "tweaking-tuning" was required to obtain the ultimate performance. More recently, PSPL has added the capability of designing and manufacturing it's own custom designed semiconductors. These include NLTLs and MMICs.

Designing it's own MMICs has allowed PSPL to now offer a whole new line of picosecond pulse generators capable of operating at GHz rep. rates. The key, custom designed, element required is that of the pulser's output amplifier

stage. Most all of the internal logic required to establish the basic pulse parameters of rep. rate, delay, duration and polarity can be accomplished with commercial, off-the-shelf, digital logic MMICs. What is not readily available commercially, are digital/analog output amplifier MMICs which provide adjustable output amplitudes larger than typical logic levels with adjustable baseline offsets.

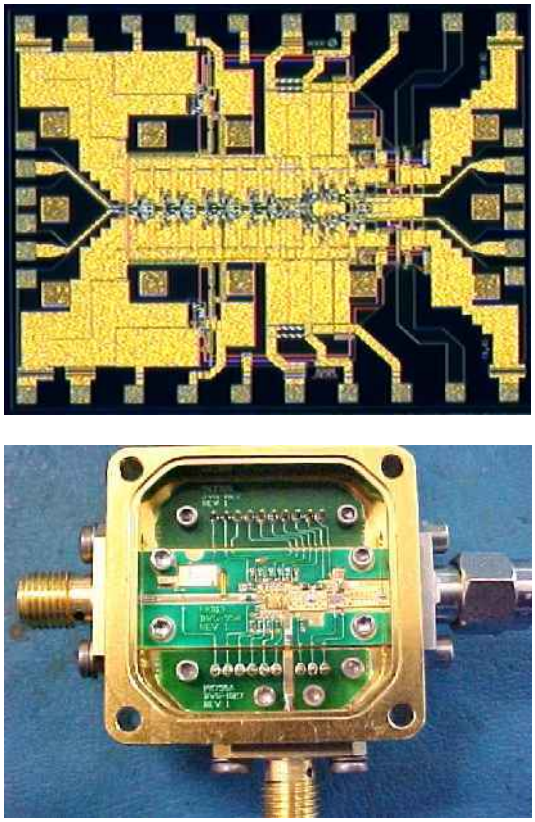

Fig. 14 PSPL custom designed Ultra-Broadband, 25 GBit/s, 2 V, 20 ps rise/falltime, Amplifier, MMIC.

The performance of PSPL's MMICs far exceed that of what was available using discrete Si transistors, described earlier. Instead of MHz max. rep. rates, PSPL's MMICs are capable of operating at GHz rep. rates. With current semiconductor fabrication technology and different materials, monolithic transistors with much smaller dimensions and much higher bandwidths are now possible compared to the old discrete transistors of the 60's. In most cases, the basic amplifying or switching element used in the MMICs is still the emitter coupled, differential amplifier shown in Fig. 4. The actual circuits used in PSPL's MMICS are considerably more complex.

To design custom MMICs, PSPL's engineers use the latest in CAD design tools to conceptualize, simulate, and layout semiconductor masks and pc board layouts. Fig. 14 shows one of PSPL's MMICs. Using such MMICs and CAD tools has dramatically reduced the need for pre-screening, hand selection of critical components, and hand "tweaking-tuning" in PSPL's newer products.

PSPL sells both complete GHz pulse/pattern generators and also GHz amplifiers which use PSPL's custom designed MMICs. PSPL's newest, model 12020 pulse/pattern generator is capable of operating at 1.6 GHz with 2.5 V, 125 ps rise/falltime pulses. See Fig. 2. PSPL's new programmable pulse/pattern amplifier is capable of operating at 25 GHz with 2 V, 20 ps rise/falltime pulses. See Figs. 3 & 14. It will be the output amplifier stage for several forthcoming new, even higher data rate, pulse/pattern generators.